	Туре	L #	Hits	Search Text	DBs	Time Stamp
	IS&R	Li	ΙŪ	(("4577215") or ("5266559") or ("4357685") or ("5287536") or ("5414.337") or ("4191444") or ("4597000") or ("5187683") or ("5216269") or ("5694445")).PN.	USPAT; US-PGPUB	2002/07/12 09:30
2		L2	3 9	(("5879932") or ("9373072") or ("33,36183") or ("3433137") or ("4433331") or ("4368739") or ("505353") or ("583343") or ("583343") or ("583343") or ("583343") or ("583343") or ("583343") or ("5844356") or ("5854356") or ("5854356") or	USPAT; US-PGPUB	2002/07/12 09:30
3	BRS	L6	12	5 not(2 or 1)	USPAT; US-PGPUB	2002/07/12 09:43
4	IS&R	L5	:	(("5070-32") or ("5095344") or ("5015541") or ("50134063") or ("5013401") or ("5013401") or ("5012760") or ("6002760") or ("4002656") or ("5043940") or ("5043940") or ("5043940") or ("50551881")).PN.	USPAT; US-PGPUB	2002/07/12 09:43

Document ID Issue Date	Issue Date		Pages	Title	Current OR	Current XRef	Inventor
US 5216269 A 1 00001 13 PRICT	1 20t-01 13		Elect:	.5	57/318	257/320; 305/185.3; 365/185.31	Middelhogk, Jan et al.
3) 33 15 00 25 	3) 33 15 00 25 	/	Dual Wo alterak gate me	Fual word line, electrically alterable, nonvolatile floating gate memory device		365/185.14; 365/185.18	Stewart, Roger G. et al.
Bi tufing 14 saing curret	method 14 saing 14 curren	Method using curre	Method using curren	d for reading 2-bit ETOX cells gate indo od drain leakage it		365/185.26	761, Mil. Las et al.
US FILLOU BL - (1040) II INDE the sa	:1 :0 :0 :0 :0 :0 :0 :0 :0 :0 :0 :0 :0 :0		Nonvol ter pr the sa	Nonvolatile meaning sell and methodier brogramming and, or verifying the same	i	365/185.03; %7.'.er.2; 365/185.22; 365/185.26	Their Weeng Lim
Us 6034892 A009307 23 fir pic	44	4	Nonvola f:r prc the sam	Nonvolatile memory cell and method fir programming and/or vellfying the same	365/185.14	365/185.01; 365/185.28	det, Weeng Lim
US 5751635 A TOPUELE 79 Read Ci	Read of Table Cells	Read c	Read ci	ircuits for analog memory	305/185.13	327/93; 327/94; 365/185.03; 365/185.2; 365/185.2;	Wohy, Sau C. et al.
US 5387534 A 19950207 11 non-vo	Method 19950207 11 non-vo array cells	Method non-vo array cells	Method non-vo array cells	of forming an array of clatile sones memory cells and of non-violatile sones memory	438/287	438/296) 438/296) 438/386	Prall, Kirk
US 5218569 A 19930608 23 Electr	19930608 23 Electr	Electr	Electr	ically alterable non volatile with n bits per memony cell	565/185.21	365/185.19; 365/185.2; 365/185.22; 365/186; 365/186;	Banks, Gerald T

Docu	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Inventor
E4 52759 kg	A BI		37	state memory	186.00	365/185; 365/195; 365/185;	Guterman, Parrel C. et al.
11:1 5851	H I H	1.981222	x 	Method of making monos flash memory for multi-level logic	438/261	438/208; 438/298	Lin, Ruel: et al.
UG 531342	64) 77) 73) 87)	19990517	(A) (O)	EEPROM with aplit gate coupre wide injection	00 00 00 00 00 00 00 00 00 00 00 00 00		Guterman, Lann.
akazus sa	4 22 4	\$ 1 21 12 15 5 5 7 1	4 .	Multistate FFprom tead and Wiltericuits and techniques	365/185.03	365/184; 365/185,33; 365/189,47; 365/195; 365/201	Mehrotra, San ay et al.
5605 SA	244 ⊅	0.1 2000 0.2 6.5 7.7	ط ون ا	Highly compact EFROM and flash EEPROM devices		257/324, 257/488; 365/188,04; 365/188,04; 365/188,04; 365/188,22; 365/188,21; 365/188,3; 365/188,3;	Hararı, Eliyahou
. ២០១ ន០	V 0435408	19910827	F ₁	Flash EEPROM memory systems having multistate storage reiis	8/ 	365/185.09; 365/185.11; 365/185.12; 365/185.2; 367/185.2; 365/185.25; 365/185.33; 365/185.33;	Harari, Eliyahou

	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Inventor
	::5 5838041 A	14981117	15	Nonvolatile sendencharter memory device having memory cell transister to 1803 with fisch region acting as a charge carrier injecting region	7 P	277.326	Sakagamı, Ellı et al.
: 1	. 5054508 A	20470701	7	:	2577324	257/225;	Makar, Hitemobu
m	1;: 4461527 A	1 2 4 1 1 0 8	30		.577325	257/326; 257/344; 257/340; 365/178;	Chen, Yung J. et al.
7	4342039 A	542099 A 1 .c. 0727	·v	Flentrically enamble programmable MMOS read only memory	365/104	2577.326; -577.326;	Fur, Thang Flang
5	US 4057820 A	19771108	: v	Dual gate MNOS transistor	257/326	146/EIG.156	Gallagher,
9	US 3925+04 A	19751209	17	Structure of and the method of professing a semiconductor matting or MNOS memory elements	-57/320	320/106	frichl, James Ronald et al.

Sec Con